Listing of Claims:

1. (Currently Amended) An integrated circuit comprising:

a two-dimensional pyramid filter architecture of an order 2N-1, where N is a positive integer greater than three, the two-dimensional pyramid filter architecture of order 2N-1 including,

one-dimensional pyramid filters of order 2N-1,

a first summer circuit; and

a second summer circuit;

said two dimensional pyramid filter architecture of order 2N-1, in operation, capable of producing, on respective clock cycles, at least the following:

a pyramid filtered output signal corresponding to the summation by the first summer circuit of output signals produced by four one-dimensional pyramid filters of order 2N-1; and

a pyramid filtered output signal corresponding to an output signal produced by summing signal sample matrices of order [2(N-1)-1] in the second summer circuit;

wherein the respective pyramid filtered output signals in said two dimensional pyramid filter architecture are summed by [[the]] a third summer circuit on respective clock cycles of said two dimensional pyramid filter architecture.

2. (Previously Presented) The integrated circuit of claim 1, wherein N is four; and

wherein said two dimensional pyramid filter architecture of order seven, in operation, capable of producing, on respective clock cycles, the pyramid filtered output signals corresponding to the summation of four signal sample matrices $P^{5x5}_{i-1,j-1}, P^{5x5}_{i-1,j+1}, P^{5x5}_{i+1,j-1}, P^{5x5}_{i+1,j+1}$.

3. (Previously Presented) The integrated circuit of claim 1, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplierless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.

4. (Previously Presented) The integrated circuit of claim 1, wherein said one-dimensional pyramid filters comprise other than one-dimensional multiplierless pyramid filters.

5. (Currently Amended) The integrated circuit of claim 1, wherein ~~said output signals produced by a plurality of one-dimensional pyramid filters being~~ the first summer circuit sums the output signals produced by eight one-dimensional pyramid filters of order five.

6. (Original) The integrated circuit of claim 5, wherein, of the eight one-dimensional pyramid filters of order five, four are applied row-wise and four are applied column-wise.

7. (Previously Presented) The integrated circuit of claim 5, wherein the eight one-dimensional pyramid filters of order five comprise eight one-dimensional multiplierless pyramid filters of order five.

8. (Previously Presented) The integrated circuit of claim 7, wherein, of the eight one-dimensional multiplierless pyramid filters of order five, four are applied row-wise and four are applied column-wise.

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Currently Amended) A method of filtering an image using a two-dimensional pyramid filter architecture of order 2N-1, where N is a positive integer greater than three, the two-dimensional pyramid filter architecture of order 2N-1 including one-dimensional pyramid filters of order 2N-1, said method comprising:

summing, on respective clock cycles of said two dimensional pyramid filter architecture, the following:

pyramid filtered output signals corresponding to output signals produced by four one-dimensional pyramid filters of order 2N-1; and

a pyramid filtered output ~~signals~~ signal corresponding to the summation of signal sample matrices of order [2(N-1)-1].

13. (Cancelled)

14. (Previously Presented) The method of claim 12, wherein N is four; and

wherein the signal sample matrices comprise four signal sample matrices $P^{5x5}_{i-1,j-1}, P^{5x5}_{i-1,j+1}, P^{5x5}_{i+1,j-1}, P^{5x5}_{i+1,j+1}$.

15. (Previously Presented) The method of claim 12, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplierless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.

16. (Currently Amended) An article comprising: a storage medium, said storage medium having stored thereon instructions, that, when executed result in filtering an image using a two-dimensional pyramid filter architecture of order 2N-1, the two-dimensional pyramid filter architecture of order 2N-1 including one-dimensional pyramid filters of order 2N-1, where N is a positive integer greater than three, by:

summing, on respective clock cycles of said two dimensional pyramid filter architecture, the following:

pyramid filtered output signals corresponding to output signals produced by four one-dimensional pyramid filters of order 2N-1; and

a pyramid filtered output ~~signals~~ signal corresponding to the summation of signal sample matrices of order [2(N-1)-1].

17. (Cancelled)

18. (Previously Presented) The article of claim 16, wherein N is four; and

wherein the signal sample matrices comprise four signal sample matrices $P^{5x5}_{i-1,j-1}, P^{5x5}_{i-1,j+1}, P^{5x5}_{i+1,j-1}, P^{5x5}_{i+1,j+1}$.

19. (Previously Presented) The article of claim 16, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplierless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.

20. (Previously Presented) An image processing system comprising:

an image processing unit to filter scanned color images;

said image processing unit including at least one two-dimensional pyramid filter architecture;

said at least one two-dimensional pyramid filter architecture comprising:

a two-dimensional pyramid filter architecture of an order 2N-1, where N is a positive integer greater than three, the two-dimensional pyramid filter architecture of order 2N-1 including one-dimensional pyramid filters of order 2N-1;

said two dimensional pyramid filter architecture of order 2N-1, in operation, capable of producing, on respective clock cycles, at least the following:

a pyramid filtered output signal corresponding to the summation of output signals produced by four one-dimensional pyramid filters of order 2N-1; and

a pyramid filtered output signal corresponding to the summation of signal sample matrices of order [2(N-1)-1];

wherein the respective pyramid filtered output signals in said two dimensional pyramid filter architecture are summed on respective clock cycles of said two dimensional pyramid filter architecture.

21. (Cancelled)

22. (Previously Presented) The system of claim 20, wherein N is four; and

wherein the signal sample matrices comprise four signal sample matrices $P^{5x5}_{i-1,j-1}, P^{5x5}_{i-1,j+1}, P^{5x5}_{i+1,j-1}, P^{5x5}_{i+1,j+1}$.

23. (Previously Presented) The system of claim 20, wherein said one-dimensional pyramid filters comprise a sequence of scalable cascaded multiplierless operational units, each of said operational units capable of producing a different order pyramid filtered output signal sample stream.